

Features :

- * 262,144 words by 16 bits organization.
- * Fast access time and cycle time.
- * Dual CAS Input.
- * Low power dissipation.
- * Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh, Hidden Refresh and Test Mode Capability.
- * 512 refresh cycles per 8ms.
- * Available in 40-Pin 400 mil SOJ and 40/44 Pin TSOP(II)
- * Single 5.0V±10% Power Supply.
- * All inputs and Outputs are TTL compatible.
- * Extended Data-Out(EDO) Page Mode operation.

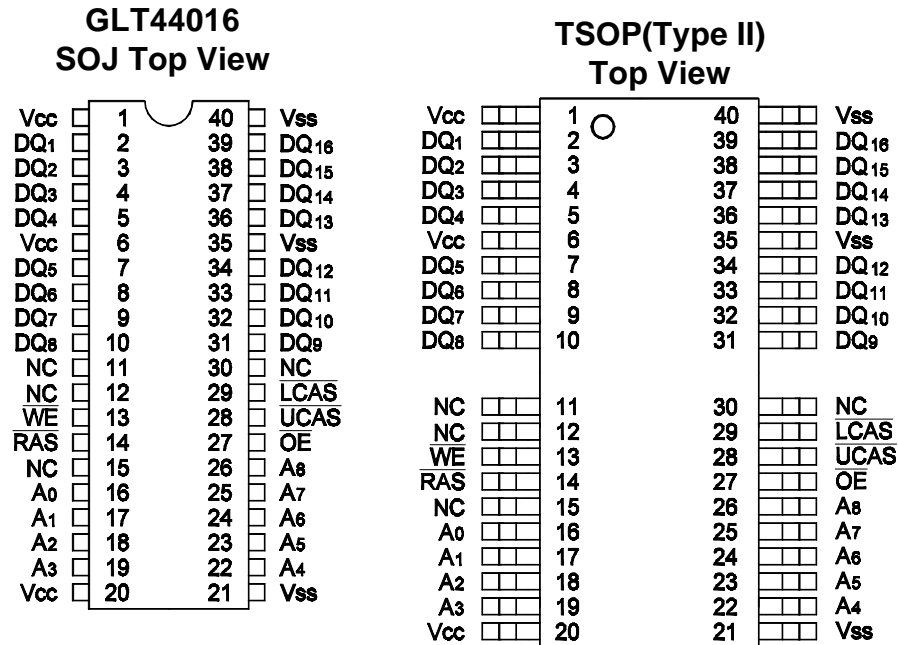
Description :

The GLT44016 is a 262,144 x 16 bit high-performance CMOS dynamic random access memory. The GLT44016 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two CAS pins. The GLT44016 has symmetric address and accepts 512-cycle refresh in 8ms interval.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 512 x 16 bits within a page, with cycle times as short as 10ns.

The GLT44016 is best suited for graphics, and DSP applications requiring high performance memories.

HIGH PERFORMANCE	25	28	30	35	40	50
Max. RAS Access Time, (t _{RAC})	25 ns	28 ns	30 ns	35 ns	40 ns	50 ns
Max. Column Address Access Time, (t _{CAA})	13 ns	13 ns	16 ns	18 ns	20 ns	25 ns
Min. Extended Data Out Page Mode Cycle Time, (t _{PC})	10 ns	10 ns	12 ns	13 ns	15 ns	20 ns
Min. Read/Write Cycle Time, (t _{RC})	45 ns	45 ns	60 ns	65 ns	70 ns	85 ns
Max. CAS Access Time (t _{CAC})	8 ns	8 ns	10 ns	11 ns	12 ns	14 ns

Pin Configuration :

Pin Descriptions:

Name	Function
$A_0 - A_8$	Address Inputs
\overline{RAS}	Row Address Strobe
\overline{UCAS}	Column Address Strobe/Upper Byte Control
\overline{LCAS}	Column Address Strobe/Lower Byte Control
\overline{WE}	Write Enable
\overline{OE}	Output Enable
$DQ_1 - DQ_{16}$	Data Inputs / Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
-0°C to +70°C
 Storage Temperature(plastic)....-55°C to +150°C
 Voltage Relative to V_{SS}-1.0V to + 7.0V
 Short Circuit Output Current.....50mA
 Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

$T_A=25^\circ\text{C}$, $V_{CC}=5V\pm 10\%$, $V_{SS}=0V$

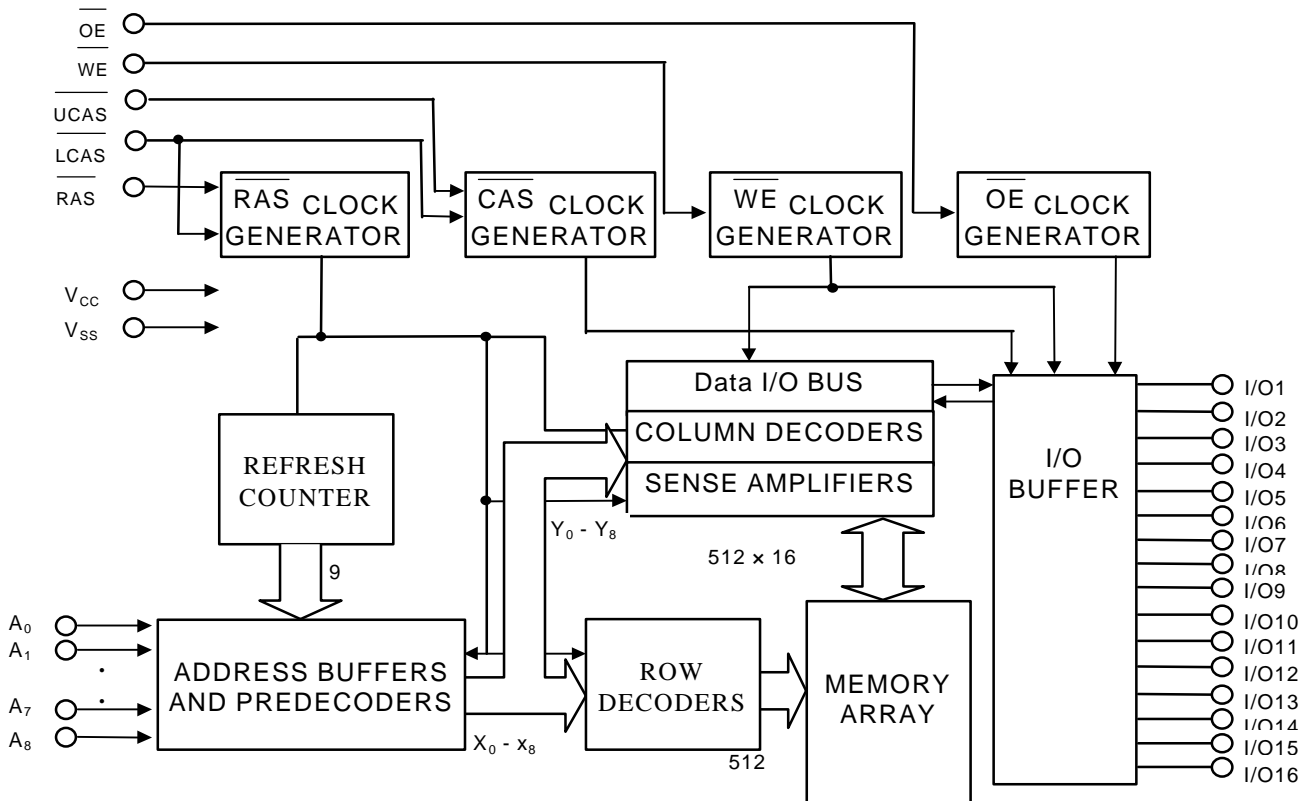
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{\text{CAS}}$ means $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
- All voltages are referenced to GND.
- After power up, wait more than 100 μs and then, execute eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ or $\overline{\text{RAS}}$ -only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table: GLT44016

Function		$\overline{\text{RAS}}$	$\overline{\text{CASL}}$	$\overline{\text{CASH}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESS	DQs	Notes
Standby		H	H→X	H→X	X	X		High-Z	
Read: Word		L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte,Data-Out Upper Byte,High-Z	
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte,High-Z Upper Byte,Data-Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	H	L	L	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L	H→L	H	L	COL	Data-Out	1
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	H→L	L	X	COL	Data-In	2
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
$\overline{\text{RAS}}$ -Only Refresh		L	H	H	X	X	ROW	High-Z	
CBR Refresh		H→L	L	L	X	X		High-Z	4

Notes:

1. These READ cycles may also be BYTE READ cycles (either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ active).
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active ($\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$).

DC and Operating Characteristics (1-2)

$T_A = 0^\circ\text{C}$ to 70°C , $V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$0V \leq V_{IN} \leq 5.5V$ (All other pins not under test=0V)		-10		+10	μA	
I_{LO}	Output Leakage Current (for High-Z State)	$0V \leq V_{out} \leq 5.5V$ Output is disabled (Hiz)		-10		+10	μA	
I_{CC1}	Operating Current, Random READ/WRITE	$t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 25\text{ns}$ $t_{RAC} = 28\text{ns}$ $t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$			270 270 250 210 190 170	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ at V_{IH} other inputs $\geq V_{SS}$				4	mA	
I_{CC3}	Refresh Current, RAS-Only	$\overline{\text{RAS}}$ cycling, $\overline{\text{UCAS}},$ $\overline{\text{LCAS}}$ at V_{IH} $t_{RC} = t_{RC}(\text{min.})$	$t_{RAC} = 25\text{ns}$ $t_{RAC} = 28\text{ns}$ $t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$			270 270 250 210 190 170	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{\text{RAS}}$ at $V_{IL}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ address cycling: $t_{PC}=t_{PC}(\text{min.})$	$t_{RAC} = 25\text{ns}$ $t_{RAC} = 28\text{ns}$ $t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$			270 270 250 210 190 170	mA	1,2
I_{CC5}	Refresh Current, CAS Before RAS	$\overline{\text{RAS}}, \overline{\text{UCAS}}, \overline{\text{LCAS}}$ address cycling: $t_{RC}=t_{RC}(\text{min.})$	$t_{RAC} = 25\text{ns}$ $t_{RAC} = 28\text{ns}$ $t_{RAC} = 30\text{ns}$ $t_{RAC} = 35\text{ns}$ $t_{RAC} = 40\text{ns}$ $t_{RAC} = 50\text{ns}$			270 270 250 210 190 170	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{\text{RAS}} \geq V_{CC}-0.2V,$ $\overline{\text{UCAS}} \geq V_{CC}-0.2V,$ $\overline{\text{LCAS}} \geq V_{CC}-0.2V,$ All other inputs V_{SS}				2	mA	
V_{IL}	Input Low Voltage			-1		+0.8	V	3
V_{IH}	Input High Voltage			2.4		$V_{CC}+1$	V	3
V_{OL}	Output Low Voltage	$I_{OL} = 4.2\text{mA}$				0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -5.0\text{mA}$		2.4			V	

Notes:

- I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC}(\text{max.})$ is measured with the output open.
- I_{CC} is dependent upon the number of address transitions specified $I_{CC}(\text{max.})$ is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.
- Specified $V_{IL}(\text{min.})$ is steady state operation. During transitions $V_{IL}(\text{min.})$ may undershoot to $-1.0V$ for a period not to exceed 20ns. All AC parameters are measured with $V_{IL}(\text{min.}) \geq V_{SS}$ and $V_{IH}(\text{max.}) \leq V_{CC}$.

AC Characteristics

 $T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, $V_{IH}/V_{IL} = 2.4/0.8\text{ V}$, $V_{OH}/V_{OL} = 2.0/0.8\text{V}$

 An initial pause of 100 μs and 8 CAS-before-RAS or RAS-only refresh cycles are required after power-up.

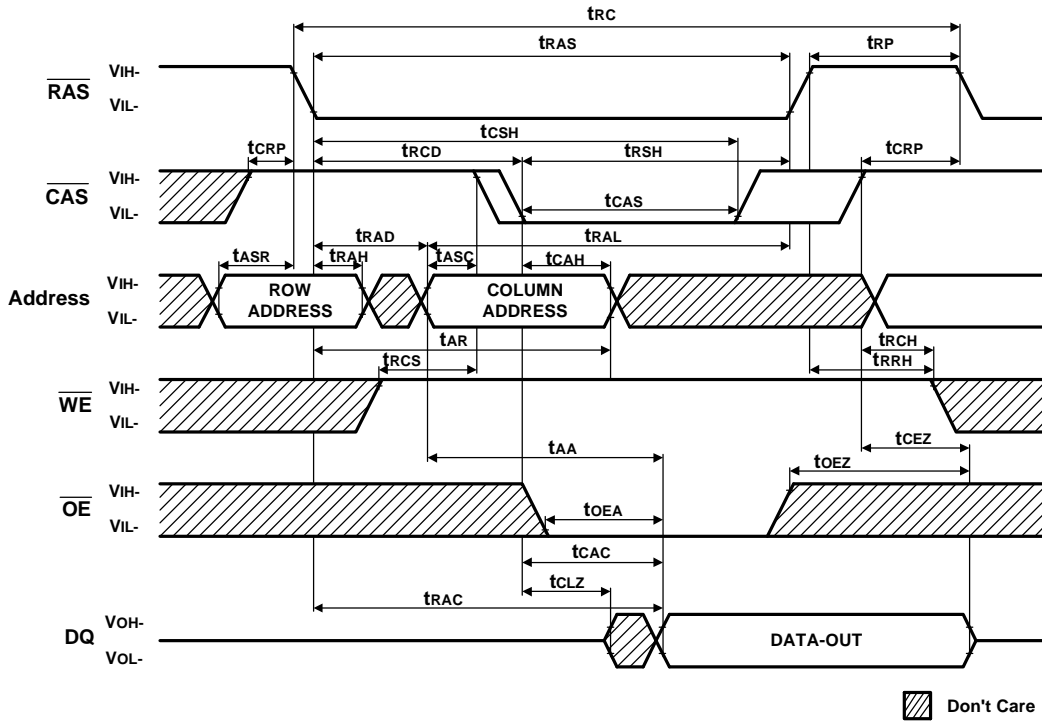
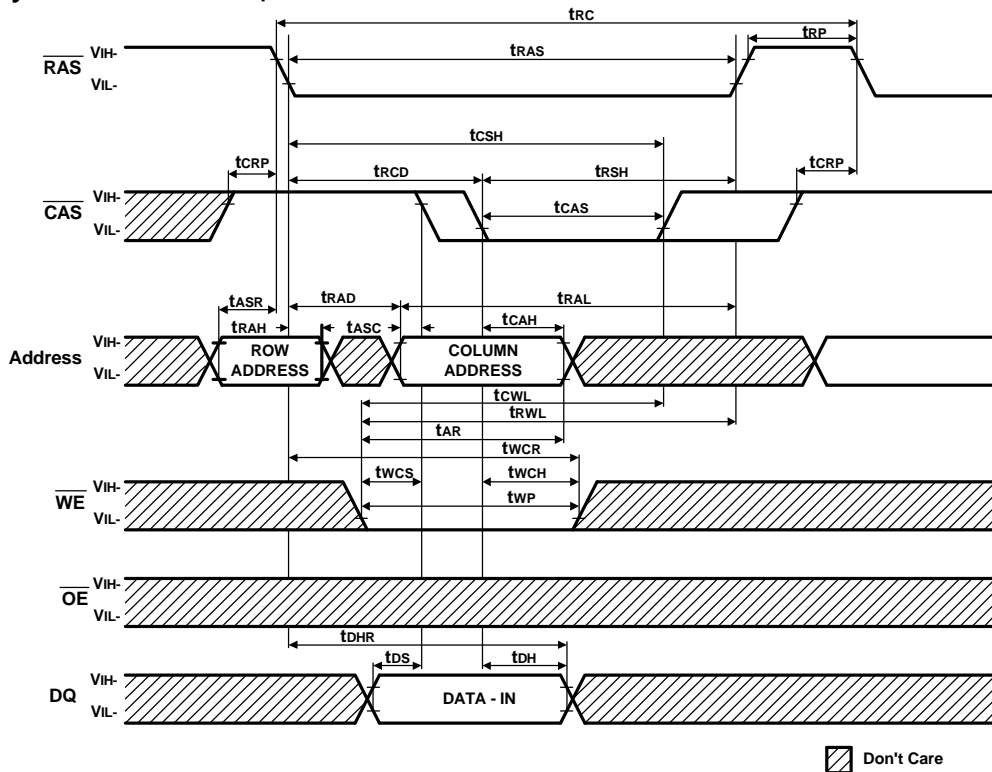
Parameter	Symbol	25		28		30		35		40		50		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Read or Write Cycle Time	t_{RC}	45		45		60		65		70		85		ns	
Read Modify Write Cycle Time	t_{RWC}	67		67		79		86		91		106		ns	
RAS Precharge Time	t_{RP}	15		15		25		25		25		30		ns	
RAS Pulse Width	t_{RAS}	25	100k	28	100k	30	100k	35	100k	40	100k	50	100k	ns	
Access Time from RAS	t_{RAC}		25		28		30		35		40		50	ns	1,2,3
Access Time from CAS	t_{CAC}		8		8		10		11		12		14	ns	1,5,10
Access Time from Column Address	t_{AA}		13		13		16		18		20		25	ns	1,5,6
CAS to Output Low-Z	t_{CLZ}		0		0	0		0		0		0		ns	
CAS to Output High-Z	t_{CEZ}	0	5	0	5	3	7	3	8	3	8	3	8	ns	
RAS Hold Time	t_{RSH}	7		7		7		8		8		8		ns	
RAS Hold Time Referenced to OE	t_{ROH}	4		4		7		8		8		8		ns	
CAS Hold Time	t_{CSH}	25		25		25		30		35		42		ns	
CAS Pulse Width	t_{CAS}	4		4		4.5		5		6		8		ns	
RAS to CAS Delay Time	t_{RCD}	10	17	10	17	10	20	11	24	12	28	13	36	ns	
RAS to Column Address Delay Time	t_{RAD}	8	12	8	12	8	14	9	17	10	20	11	25	ns	7
CAS to RAS Precharge Time	t_{CRP}	5		5		5		5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	4		4		6		7		8		9		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		0		0		0		ns	
Column Address Hold Time	t_{CAH}	4		4		5		6		6		7		ns	
Column Address to RAS Lead Time	t_{RAL}	13		13		16		18		20		25		ns	
Column Address Hold Time Referenced to RAS	t_{AR}	19		19		25		30		34		35		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		0		0		0		ns	
Read Command Hold Time Referenced to CAS	t_{RCH}	0		0		0		0		0		0		ns	4
Read Command Hold Time Referenced to RAS	t_{RRH}	0		0		0		0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	4		4		5		6		6		6		ns	
Write Command Pulse Width	t_{WP}	4		4		5		6		6		6		ns	
Write Command to RAS Lead Time	t_{RWL}	7		7		7		8		8		8		ns	
Write Command to CAS Lead Time	t_{CWL}	5		5		6		7		7		7		ns	

AC Characteristics

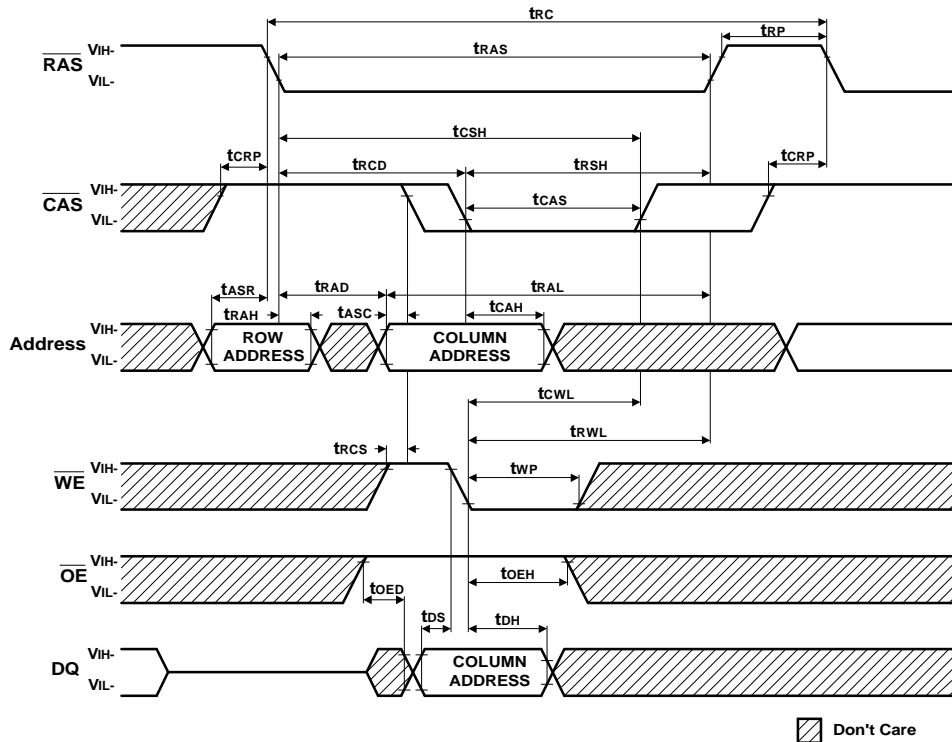
Parameter	Symbol	25		28		30		35		40		50		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t _{DS}	0	0	0	0	0		0		0		0		ns	
Data Hold Time	t _{DH}	4		4		7		8		8		8		ns	
Data Hold Time Referenced to RAS	t _{DHR}	19		19		27		32		36		37		ns	
RAS to WE E Delay Time	t _{RWD}	36		36		43		49		54		64		ns	
CAS to WE Delay Time	t _{CWD}	19		19		21		23		24		26		ns	
Column Address to WE Delay Time	t _{AWD}	24		24		27		30		32		37		ns	
RAS to CAS Precharge Time	t _{RPC}	0		0		0		0		0		0		ns	
Access Time from CAS Precharge	t _{CPA}	15		15			18		20		22		27	ns	
EDO Page Mode Cycle Time	t _{PC}	10		10		12		13		15		20		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t _{PRWC}	35		35		39		43		45		50		ns	
CAS Precharge Time (EDO Page Mode)	t _{CP}	3		3		4.5		5		6		8		ns	
RAS Pulse Width (EDO Page Mode Only)	t _{RASP}	25	100k	28	100k	30	100K	35	100k	40	100k	50	100k	ns	
Access Time from OE	t _{OEA}		8		8		10		11		12		14	ns	
OE to Data Delay Time	t _{OED}	5		5		7		8		8		8		ns	
OE to Output High-Z	t _{OEZ}	3	7	3	7	3	7	3	8	3	8	0	8	ns	
OE Command Hold Time	t _{OEH}	5		5		6		6		7		7		ns	
Data Output Hold after CAS low	t _{DOH}	4		4		5		5		5		5		ns	
RAS to Output High-Z	t _{REZ}	3	7	3	7	3	7	3	8	3	8	3	8	ns	
WE to Output High-Z	t _{WEZ}	3	10	3	10	3	10	3	10	3	10	3	12	ns	
OE to CAS Hold Time	t _{OCH}	8		8		8		8		8		8		ns	
CAS Hold Time to OE	t _{CHO}	8		8		8		8		8		8		ns	
OE Precharge Time	t _{OEP}	8		8		8		8		8		8		ns	
CAS Set-Up Time for CAS-before-RAS Cycle	t _{CSR}	5		5		10		10		10		10		ns	
CAS Hold Time for CAS-before-RAS Cycle	t _{CHR}	6		6		7		8		8		10		ns	
Transition Time	t _T	1.5	50	1.5	50	1.5	50	1.5	50	1.5	50	2	50	ns	
Refresh Period	t _{REF}		8		8		8		8		8		8	ms	

Notes:

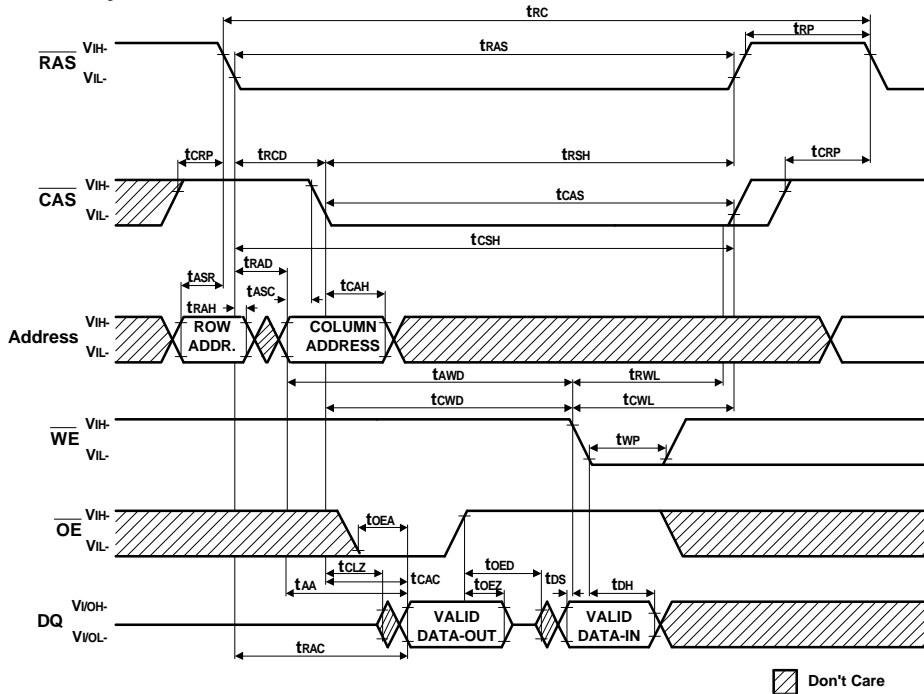
1. Measure with a load equivalent to one TTL inputs and 50 pF.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$. If t_{RCD} is greater than $t_{RCD}(\text{max.})$, access time will be t_{AA} dominant.
 3. Assumes that $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RAD} is greater than $t_{RCD}(\text{max.})$, access time will be controlled by t_{CAC} .
 4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
 5. Access time is determined by the longest of t_{CAA} , t_{CAC} and t_{CPA} .
 6. Assumes that $t_{RAD} \geq t_{RAD}(\text{max.})$.
 7. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, the access time is controlled by t_{CAA} and t_{CAC} .
 8. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters.
 9. $t_{WCS}(\text{min.})$ must be satisfied in an Early Write Cycle.
 10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.
- t_T is measured between $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$. AC-measurements assume $t_T = 1.5 \text{ ns}$.**

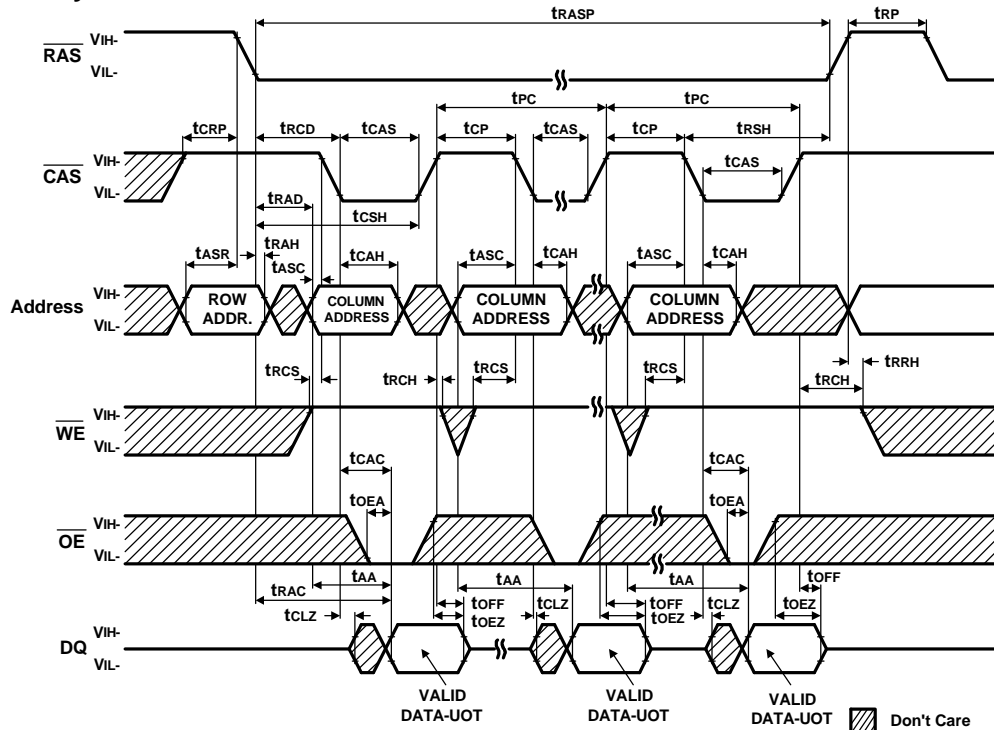
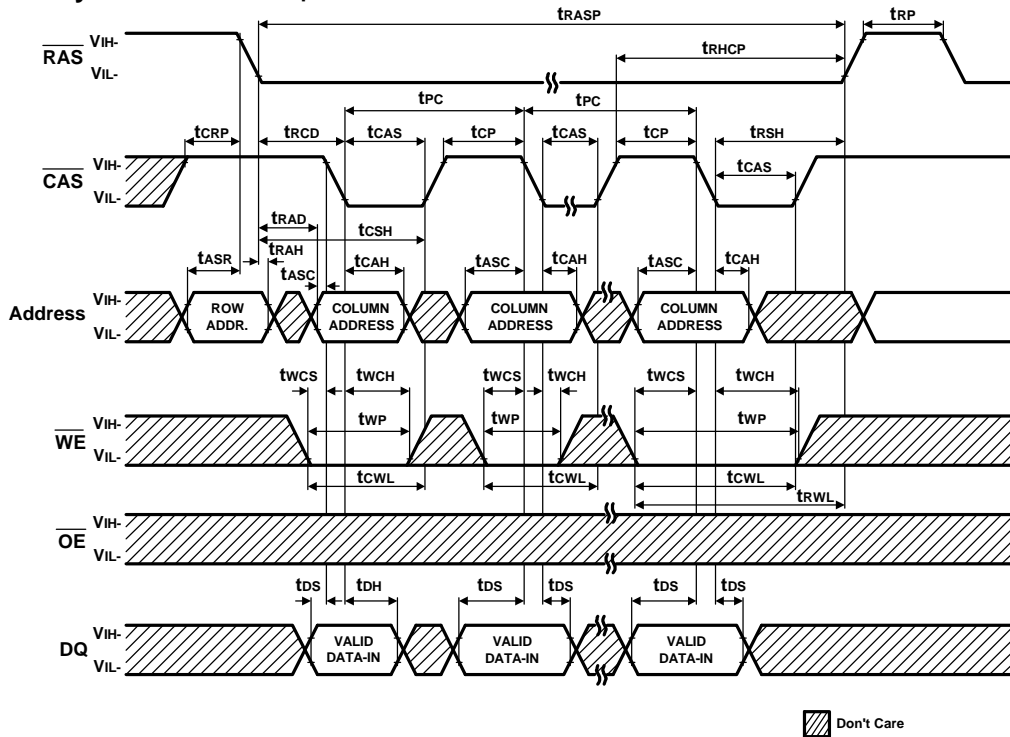
Read Cycle

Early Write Cycle NOTE : D_{OUT} = Open


Late Write Cycle (\overline{OE} Controlled Write) NOTE : $D_{OUT} = \text{Open}$

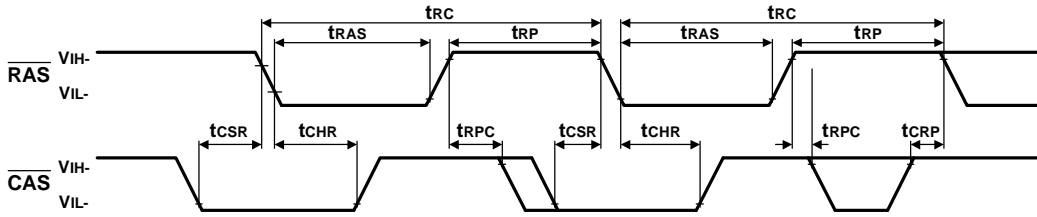


Read - Modify - Write Cycle

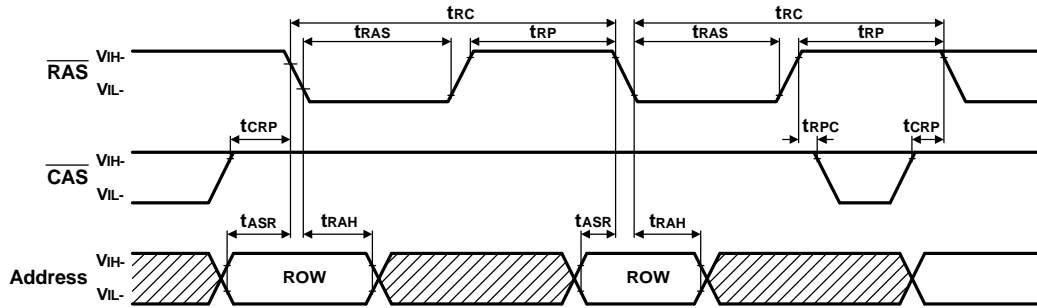


Fast Page Read Cycle

Fast Page Write Cycle NOTE : $D_{OUT} = \text{Open}$


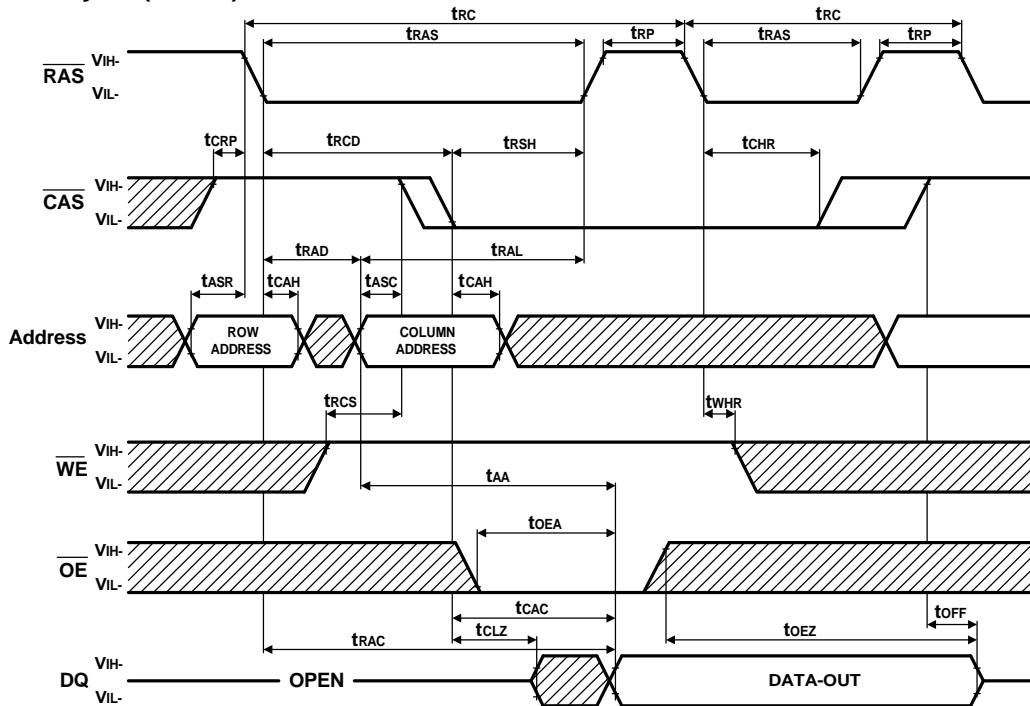
CAS Before RAS Refresh Cycle



RAS -Only Refresh Cycle

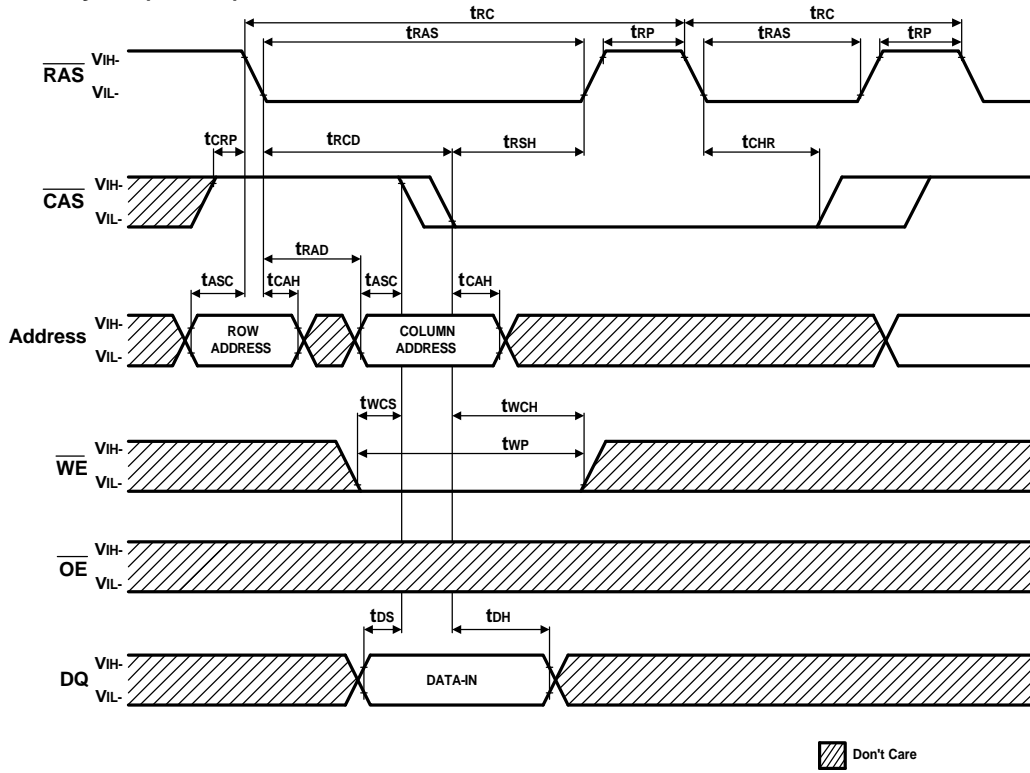


Hidden Refresh Cycle (Read)



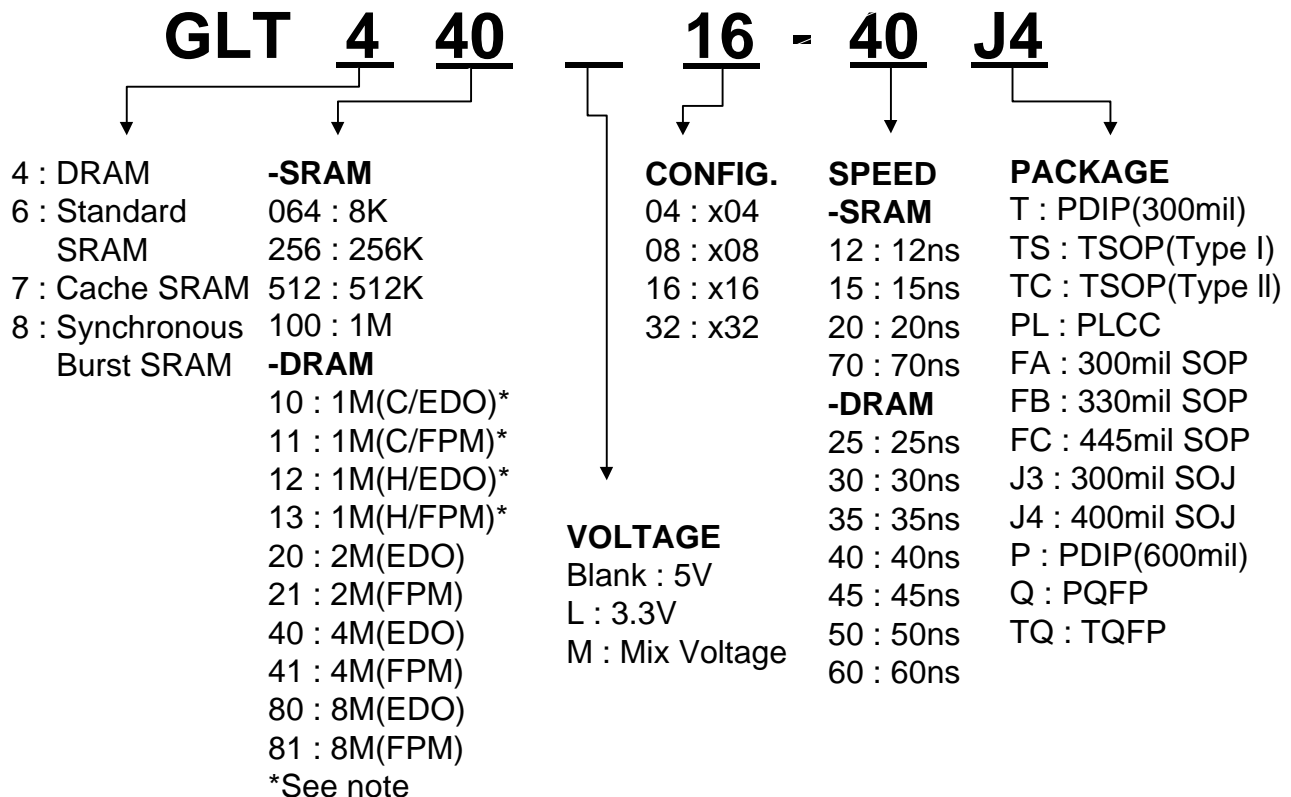
 Don't Care

Hidden Refresh Cycle (Write) NOTE : D_{OUT} =Open



Ordering Information

Part Number	SPEED	POWER	FEATURE	PACKAGE
GLT44016-25J4	25ns	Normal	EDO	40L 400mil SOJ
GLT44016-28J4	28ns	Normal	EDO	40L 400mil SOJ
GLT44016-30J4	30ns	Normal	EDO	40L 400mil SOJ
GLT44016-35J4	35ns	Normal	EDO	40L 400mil SOJ
GLT44016-40J4	40ns	Normal	EDO	40L 400mil SOJ
GLT44016-50J4	50ns	Normal	EDO	40L 400mil SOJ
GLT44016-25TC	25ns	Normal	EDO	44L 400mil TSOP
GLT44016-28TC	28ns	Normal	EDO	44L 400mil TSOP
GLT44016-30TC	30ns	Normal	EDO	44L 400mil TSOP
GLT44016-35TC	35ns	Normal	EDO	44L 400mil TSOP
GLT44016-40TC	40ns	Normal	EDO	44L 400mil TSOP
GLT44016-50TC	50ns	Normal	EDO	44L 400mil TSOP

Parts Numbers (Top Mark) Definition :


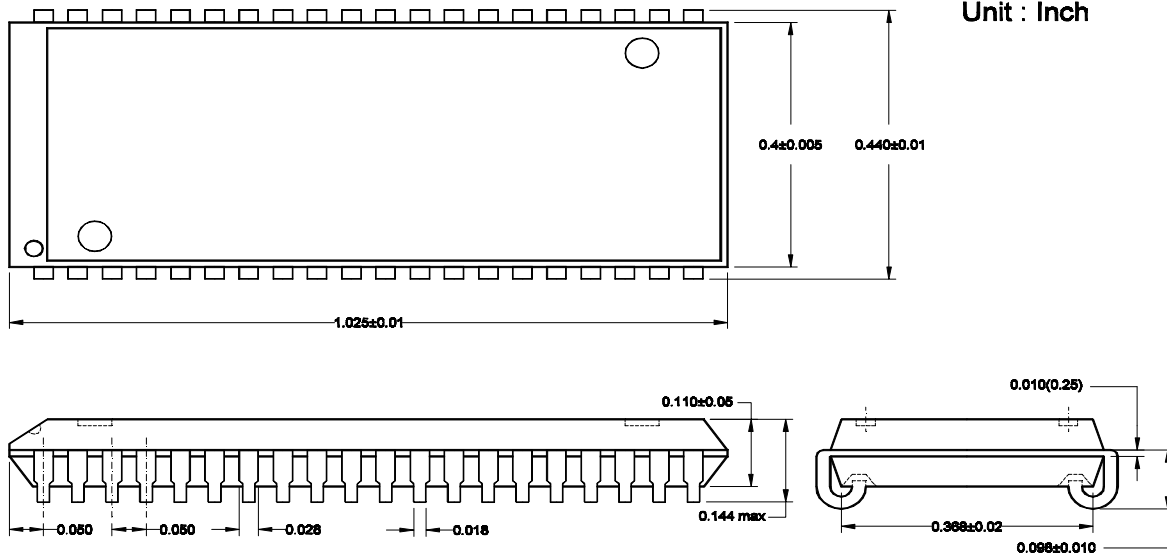
Note : C→CDROM , H→HDD.

Example :

1. GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2. GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

40/44 Lead Thin Small Outline Package SOJ



40/44 Lead Thin Small Outline Package TSOP(Type II)

